

FIG.1A

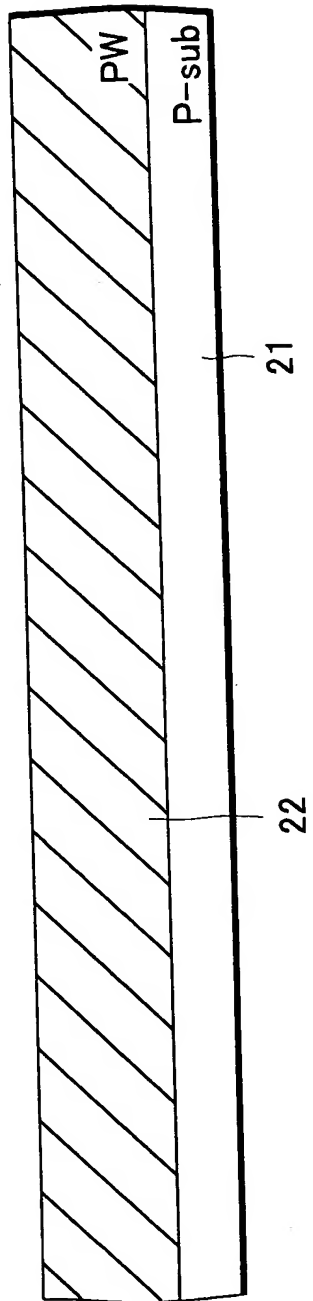
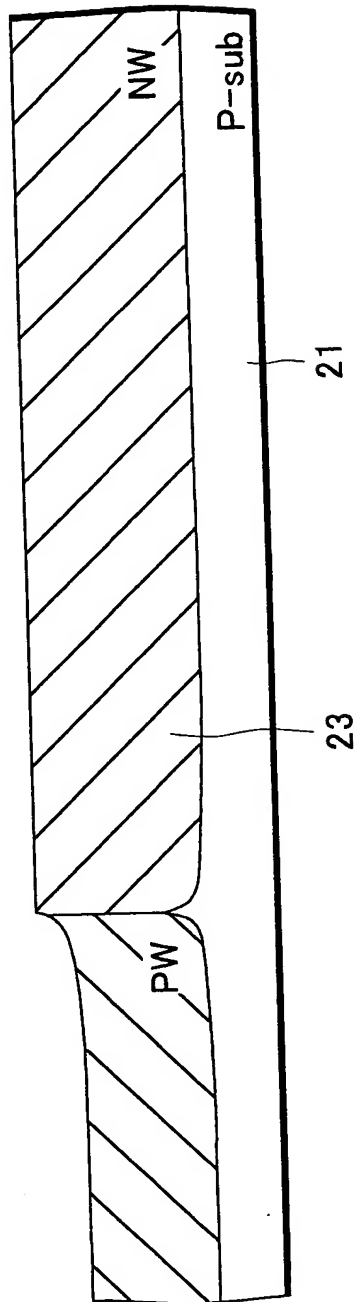


FIG.1B



**FIG.2B**

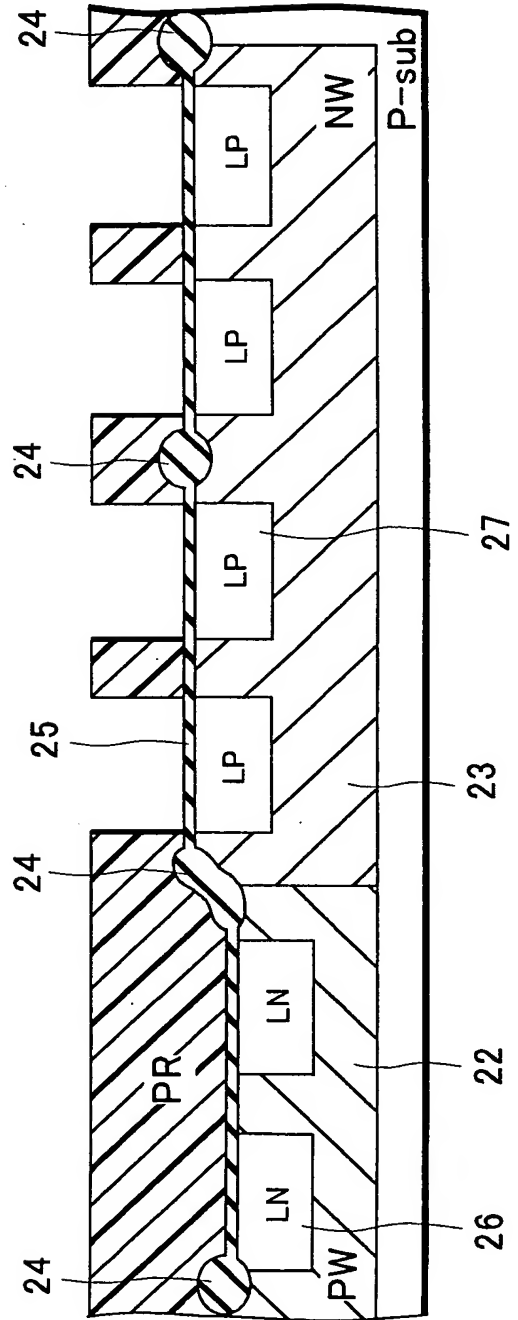


FIG.3A

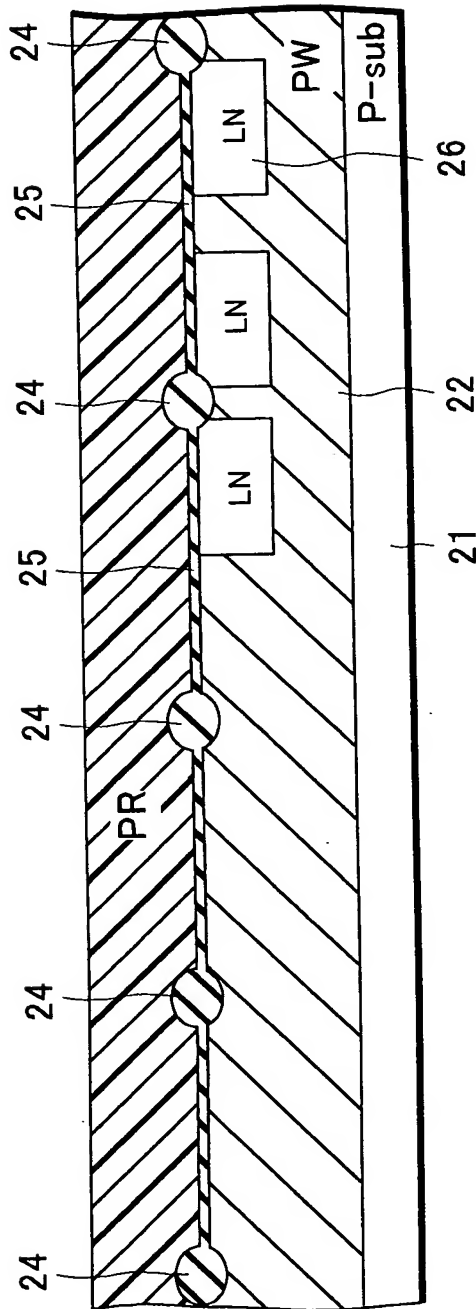


FIG.3B

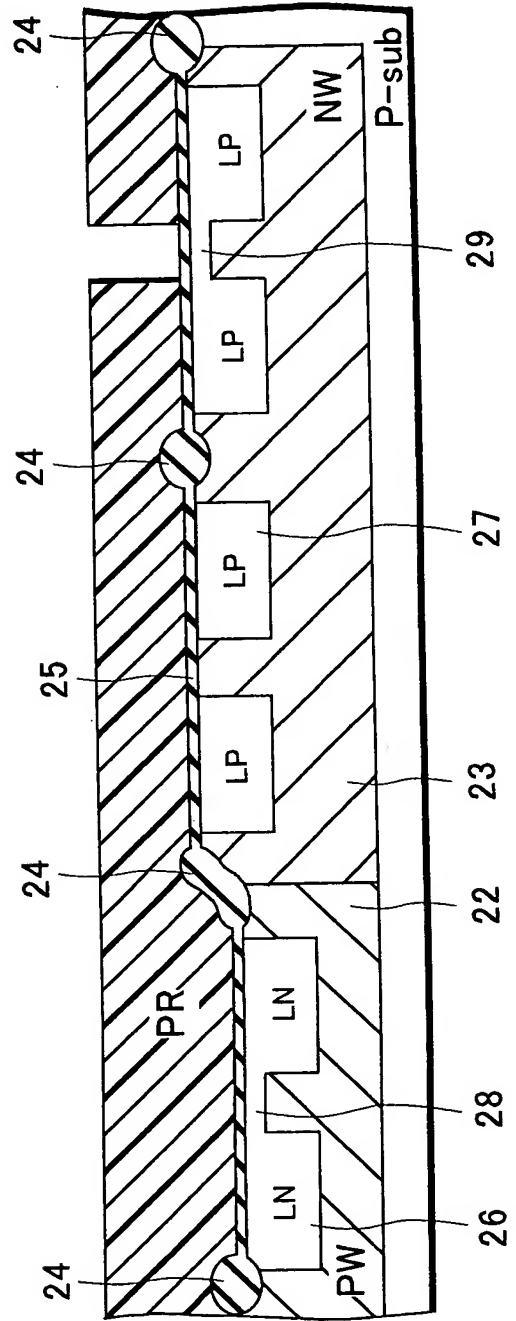


FIG.4A

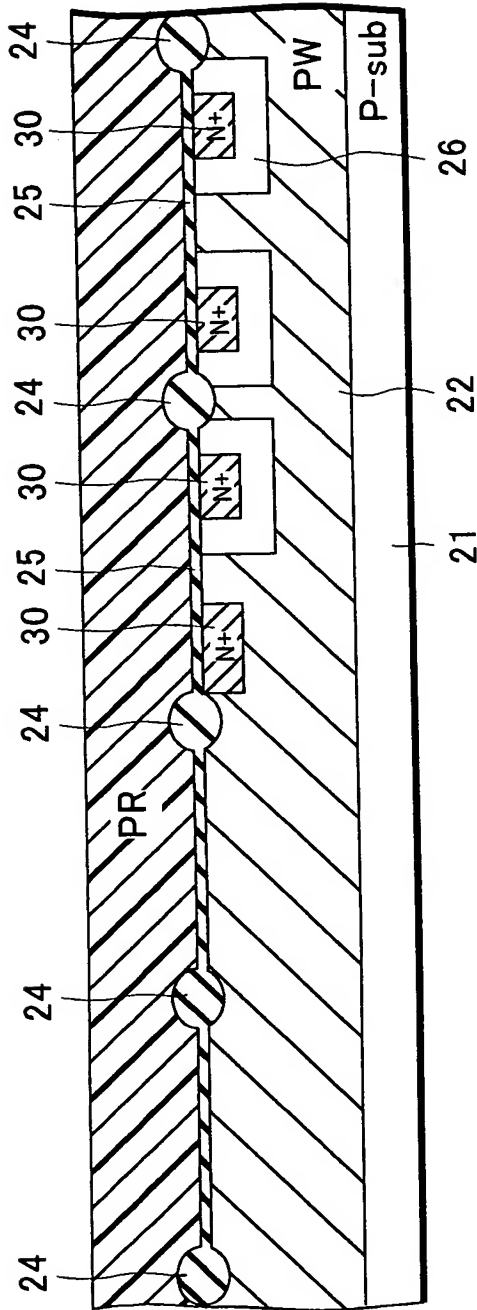


FIG.4B

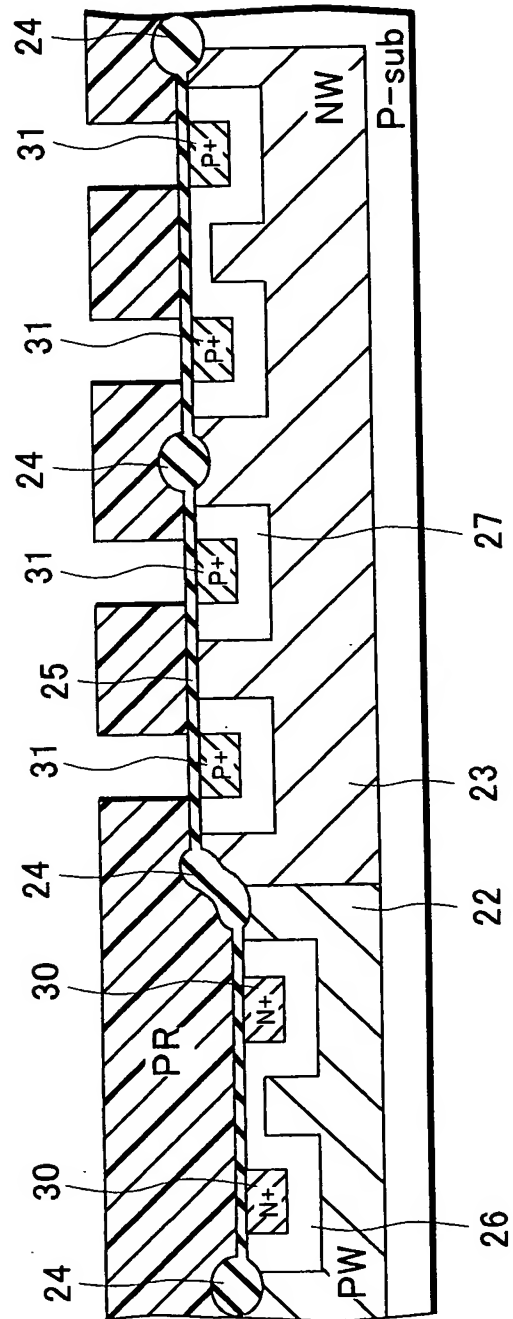


FIG.5A

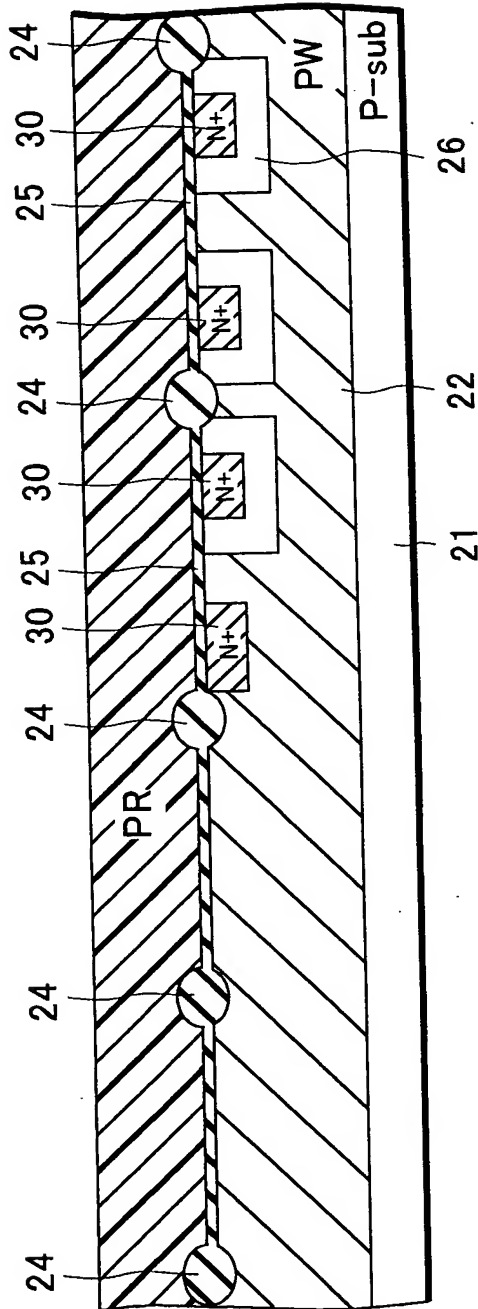


FIG.5B

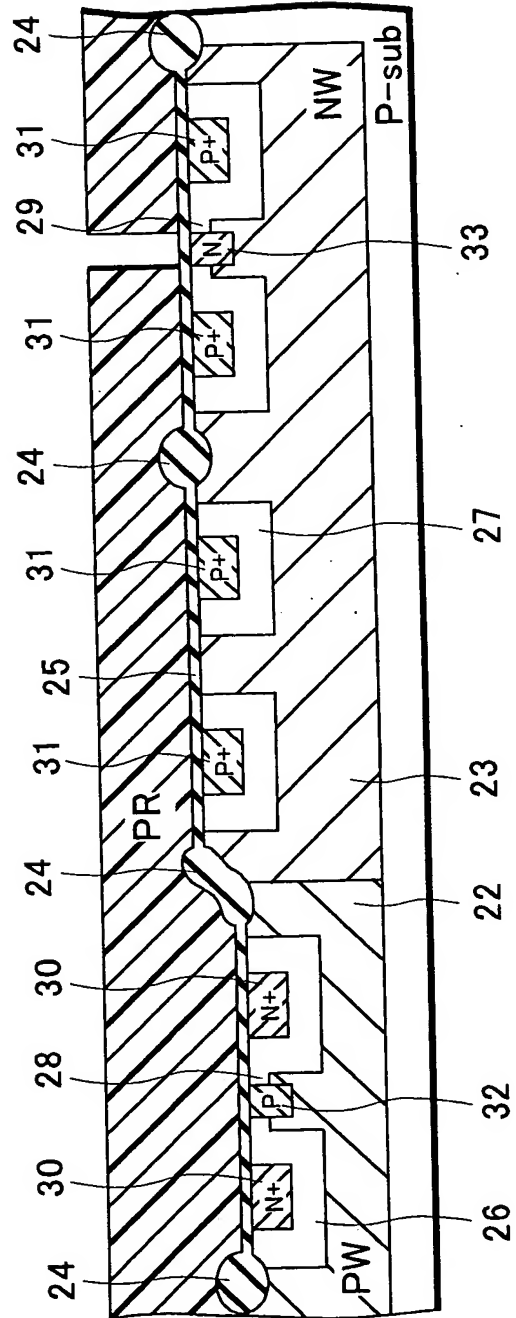






FIG. 8A

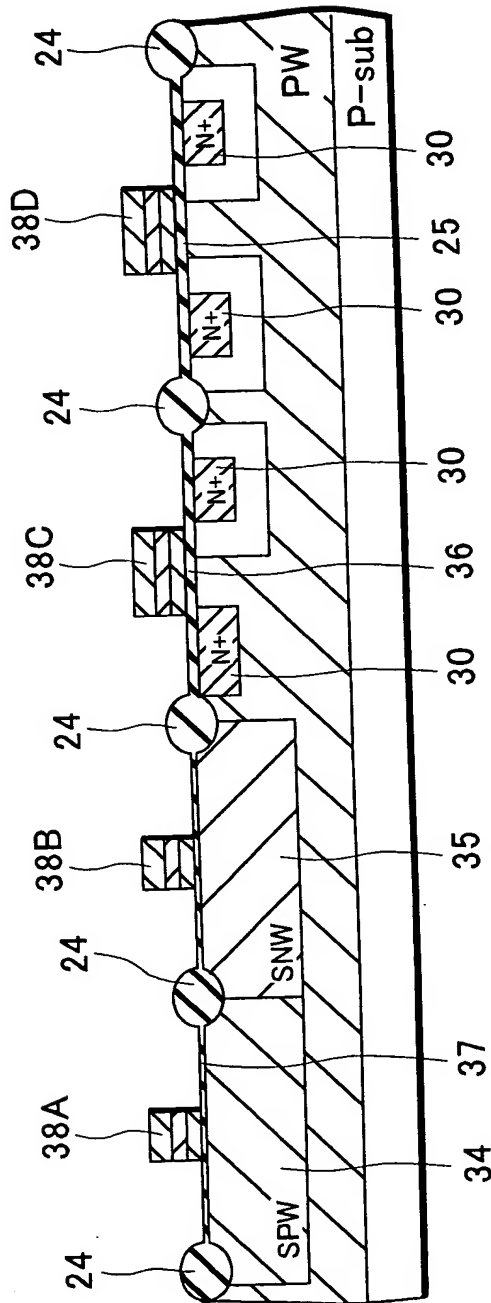


FIG. 8B

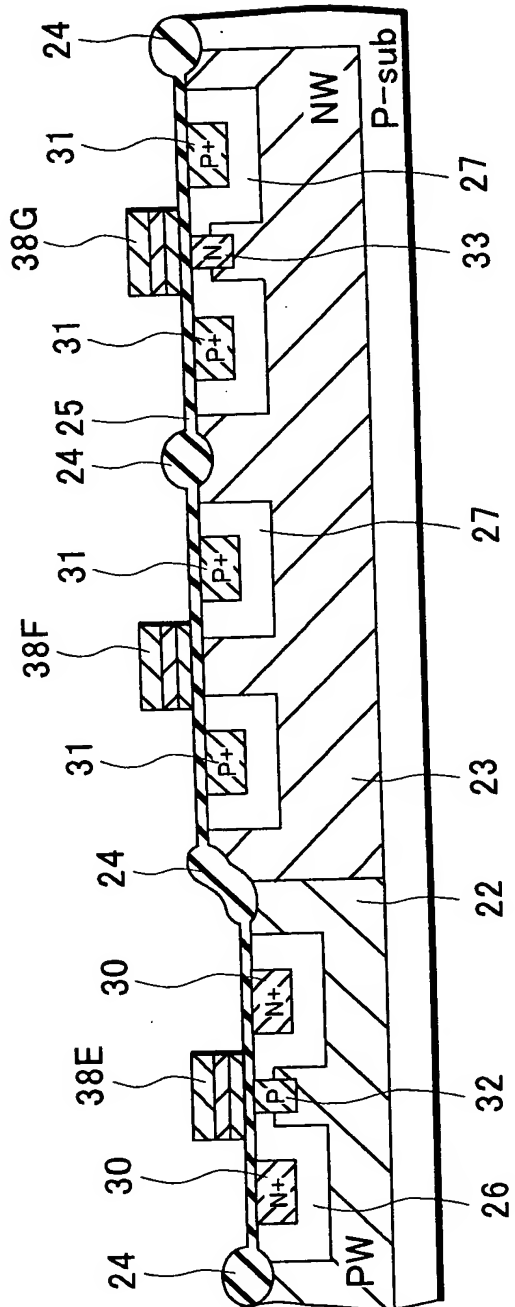




FIG.9A

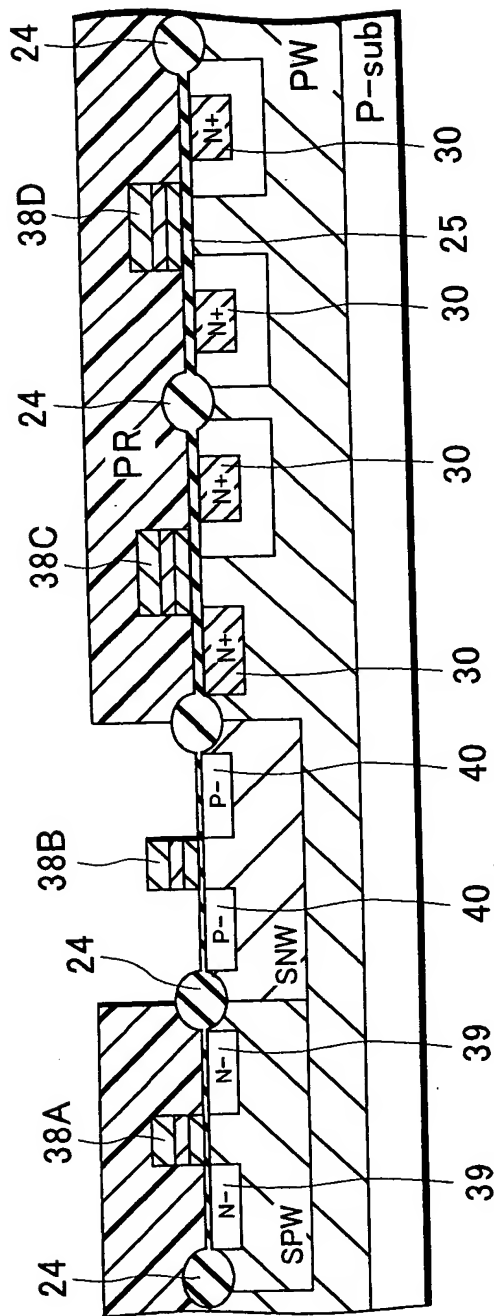
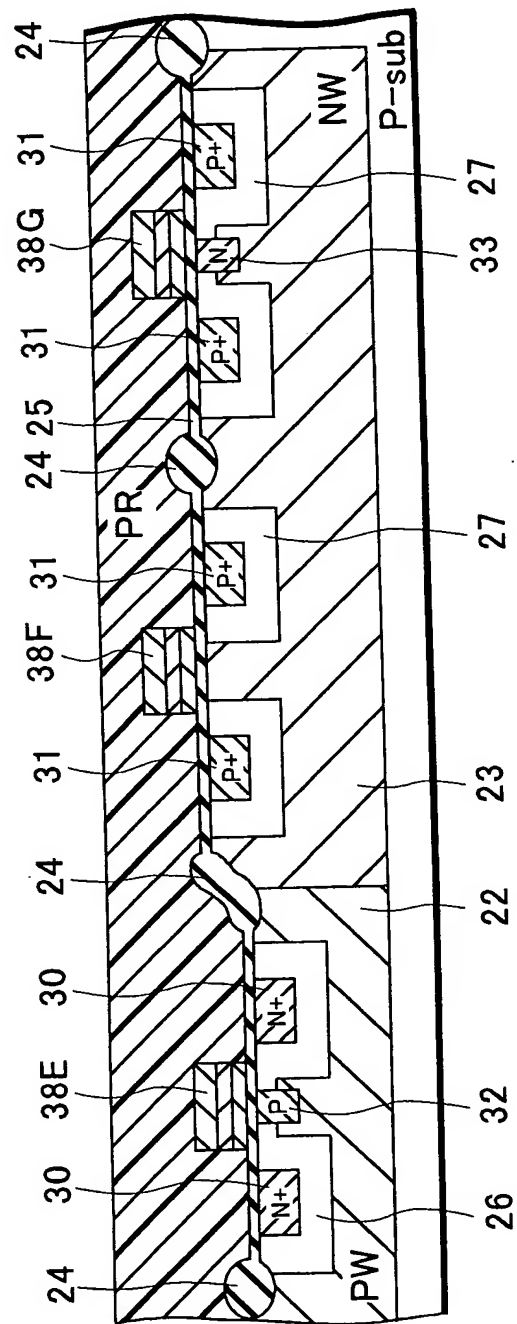


FIG.9B



This cross-sectional diagram illustrates a semiconductor device with a substrate 30. The device features a series of layers and regions: a top layer 24, a layer 38A with regions 42, 39, and 41A; a layer 38B with regions 43, 40, and 41A; a layer 38C with regions 41 and 30; and a layer 38D with regions 24 and 30. The device includes various doped regions: N+ regions (39, 42, 41A, 43, 40, 41, 30), P+ regions (41A, 43, 40, 41, 30), and P-sub regions (30). Other labeled components include SPW, SNW, PW, and PR.

This diagram shows a cross-sectional view of a semiconductor device. A central channel, labeled 24, runs horizontally through the center. The channel is flanked by two main regions: 26 on the left and 27 on the right. The channel is divided into several segments by vertical gates or barriers. These gates are labeled 23, 25, 27, 30, 31, 32, 33, 38E, 38F, 38G, and 41. The gates are made of a material labeled 'P+' (p-type dopant). The channel segments are labeled 'N+' (n-type dopant). The regions 26 and 27 are labeled 'P-sub' (p-type substrate). The regions 30 and 32 are labeled 'PW' (passivation layer). The regions 38E, 38F, and 38G are labeled 'PR' (polymer resist). The regions 30 and 32 are also labeled 'N+' (n-type dopant). The regions 30 and 32 are also labeled 'P+' (p-type dopant). The regions 30 and 32 are also labeled 'N+' (n-type dopant). The regions 30 and 32 are also labeled 'P+' (p-type dopant).

FIG.11

(A) (B) (C)

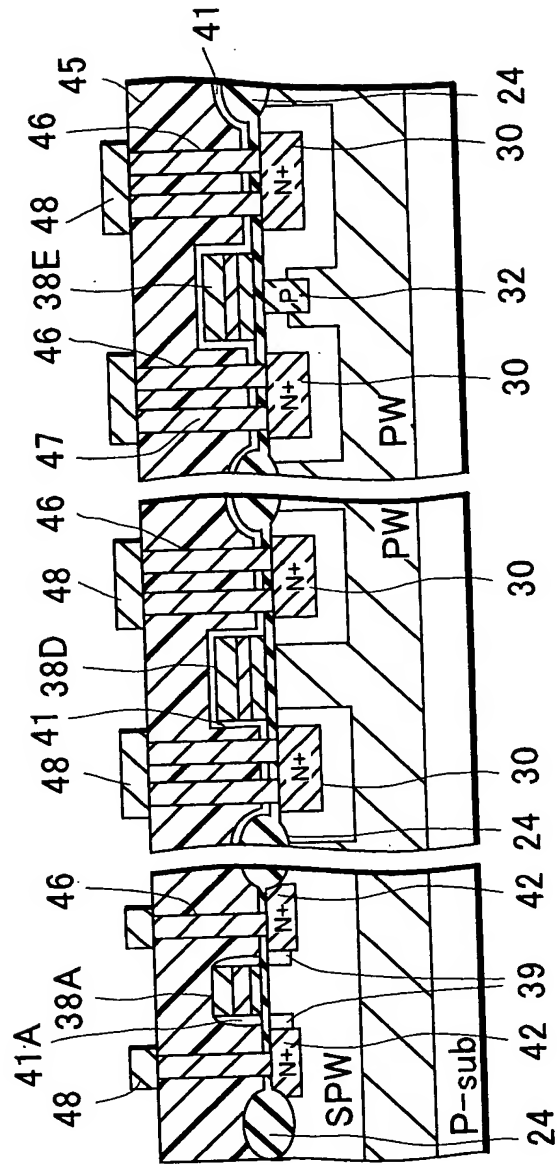


FIG. 12

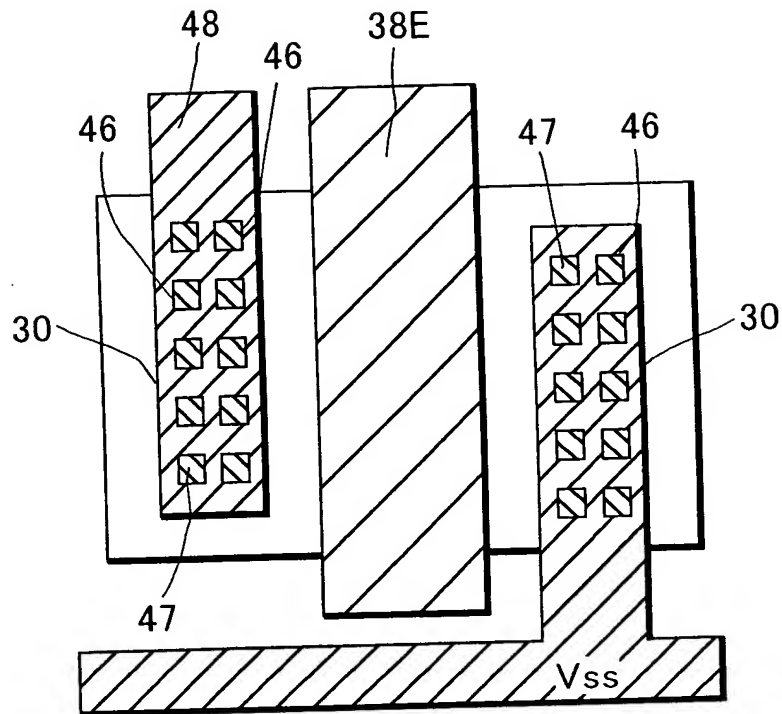




FIG.14

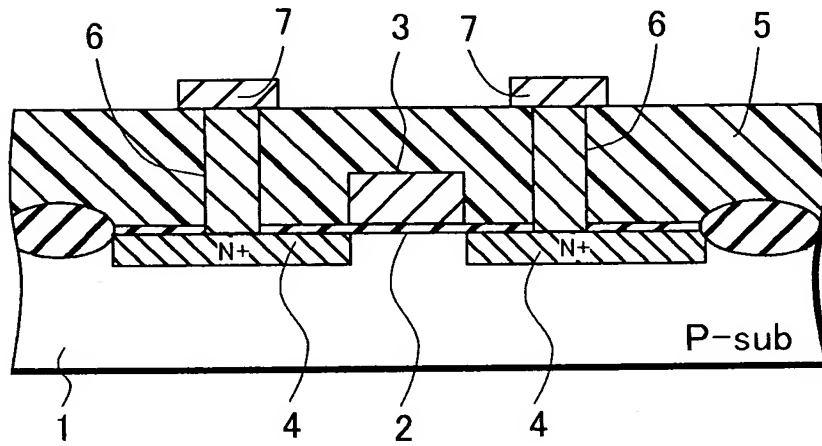


FIG.15

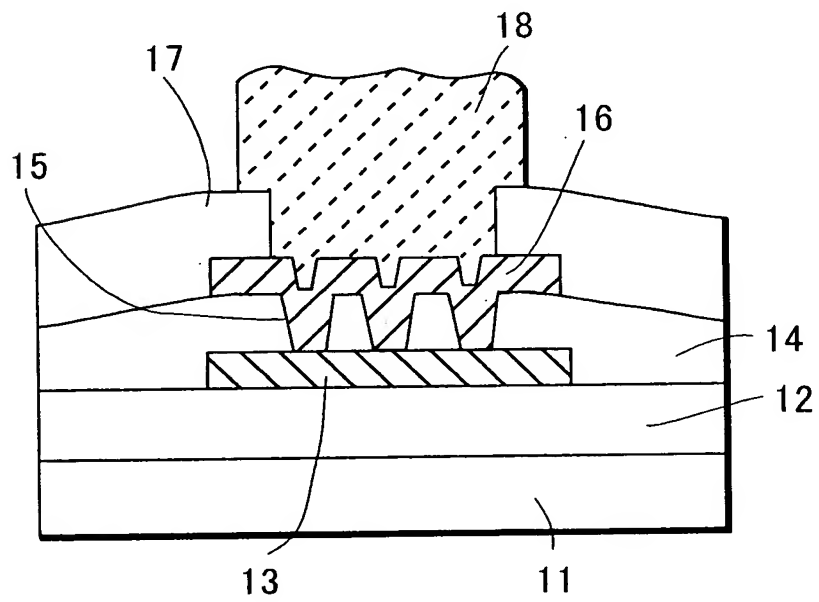


FIG. 16

